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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Question Set-4 Digital Technologies and microprocessor

Date:-06/04/2020

A. Objectives Questions:

1. The instruction that loads effective address formed by destination operand into the specified source register is
   a) LEA
   b) LDS
   c) LES
   d) LAHF
2. The instruction that loads the flag register completely from the word contents of the memory location is
   a) PUSH
   b) POP
   c) PUSHF
   d) POPF
3. The instruction that adds immediate data/contents of the memory location specified in an instruction/register to the contents of another register/memory location is
   a) SUB
   b) ADD
   c) MUL
   d) DIV
4. The instruction that supports addition when carry exists is
   a) ADD
   b) ADC
   c) ADD & ADC
   d) None of the mentioned
5. The instruction that is used for finding out the codes in case of code conversion problems is
   a) XCHG
   b) XLAT
   c) XOR
   d) JCXZ
6. The instructions that involve various string manipulation operations are
   a) branch instructions
   b) flag manipulation instructions
   c) shift and rotate instructions
   d) string instructions

7. While programming for any type of interrupt, the interrupt vector table is set
   a) externally
   b) through a program
   c) either externally or through the program
   d) externally and through the program.
8. To execute a program one should
   a) assemble the program
   b) link the program
   c) apply external pulse
   d) all of the mentioned
9. Procedures are also known as
   a) macros
   b) segment
   c) subroutines
   d) none
10. Procedures, for their execution, require
    a) input data
    b) output data
    c) constants
    d) input data or constants

B. Short Answer Types Questions:

1. What do you mean by masking the interrupt? How it is activated in 8085?
2. What is Address Bus?.
3. What is the function of program counter in 8085 processor?
4. What are the limitations of 8085 MPU?
5. Why is the data bus bi-directional?
6. What is a flag?
7. Explain the function of ALE and IO/M signals in the 8085 architecture?
8. What is pipelined architecture?
9. Specify the size of data, address, memory word and memory capacity of 8085 microprocessor
10. What are the various flags used in 8085?

C. Long Answer Types Questions:

1. Write in brief about the internal architecture of microprocessor 8086.
2. Draw the timing diagram of Memory WRITE machine cycle for 8085.
3. Explain the functions of 8085 signals.
4. Design a microprocessor system to interface an 8K × 8 EPROM and 8K × 8 RAM
5. Write an ALP for Addition of two 16 bit numbers using 8086.

Solutions:

A. Objectives Questions:

1. Answer: a
   Explanation: The instruction, LEA loads effective address and is more useful for assembly language rather than for machine language
2. Answer: d
   Explanation: POPF is pop flags to stack.
3. Answer: b
   Explanation: ADD instruction adds the data
4. Answer: b
   Explanation: ADC(Add with Carry) instruction performs the same operation as ADD operation, but adds the carry flag bit to the result
5. Answer: b
   Explanation: The translate(XLAT) instruction is used to find codes
6. Answer: d
   Explanation: The string instructions perform operations on strings such as load, move, scan, compare etc.
7. Answer: c
   Explanation: The programmer must, either externally or through the program, set the interrupt vector table for that type preferably with the CS and IP addresses of the interrupt service routine.
8. Answer: d
   Explanation: To execute a program, first assemble it, link it and then execute it. After execution, a new file RESULT is created in the directory. Then external pulse is applied to IRQ2 pin, and this will again cause the execution of ISR into the file
9. Answer: c
   Explanation: Procedures are also known as subroutines
10. Answer: d
    Explanation: Procedures require input data or constants for their execution. Their data or constants may be passed to the subroutine by the main program.

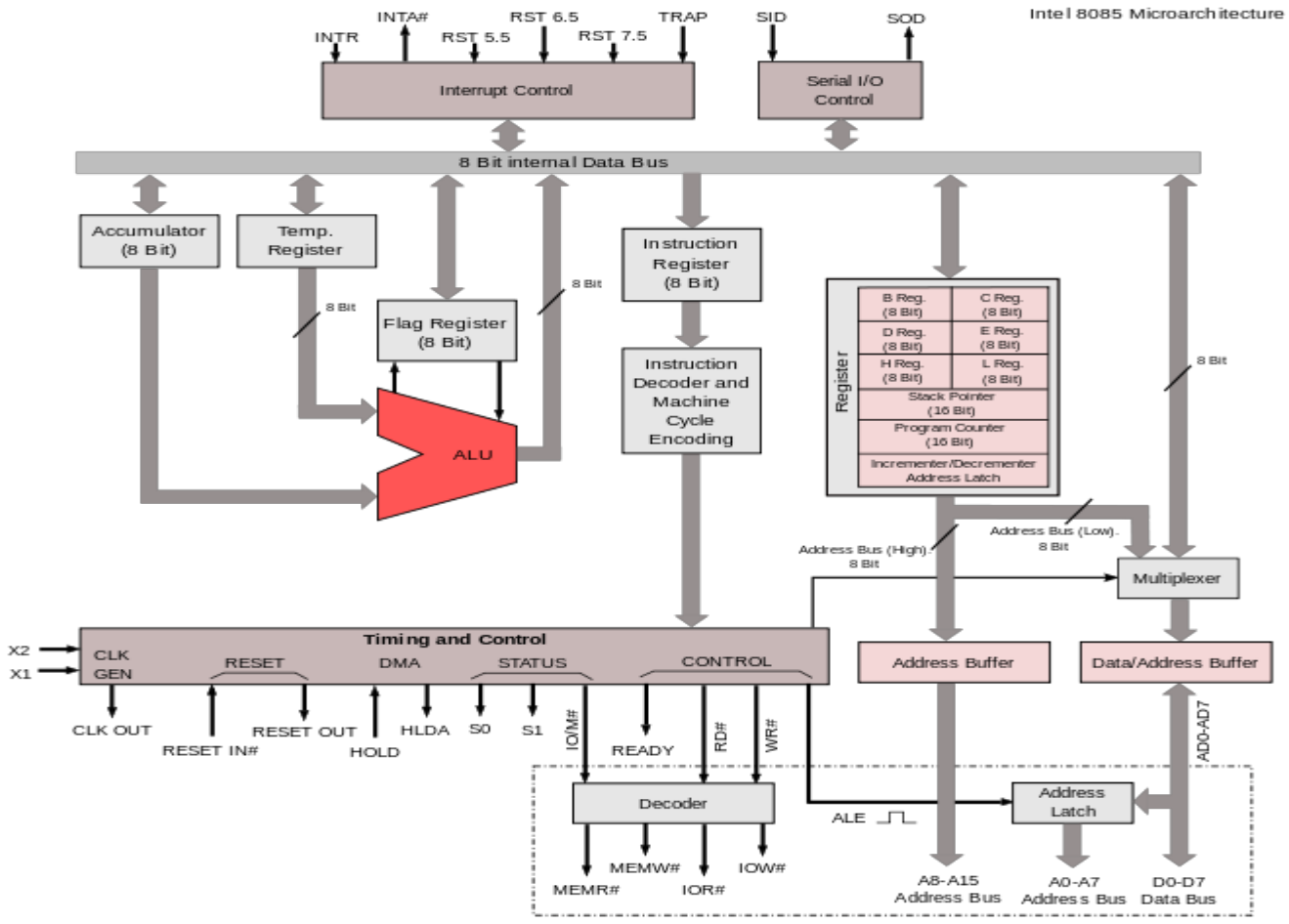
B. Short Answer Types Questions.

1. Masking is preventing the interrupt from disturbing the current program execution.When the processor is performing an important job (process) and if the process should not be interrupted then all the interrupts should be masked or disabled. In processor with multiple interrupts, the lower priority interrupt can be masked so as to prevent it from interrupting, the execution of interrupt service routine of higher priority interrupt
2. The address is an identification number used by the processor to identify or access a memory location or I/O device. It is an output signal from the processor. Hence the address bus is unidirectional.
3. The microprocessor uses this register to sequence the execution of the instructions. The function of the program counter is to point to the memory address from which the next byte is to be fetched. When a byte (machine code) is being fetched, the program counter is incremented by one to point to the next memory location.
4. i) The lower order address bus of the 8085 microprocessor is multiplexed (time shared) with the data bus. The buses need to be demultiplexed.
   (ii) Appropriate control signals need to be generated to interface memory and I/O with the 8085.

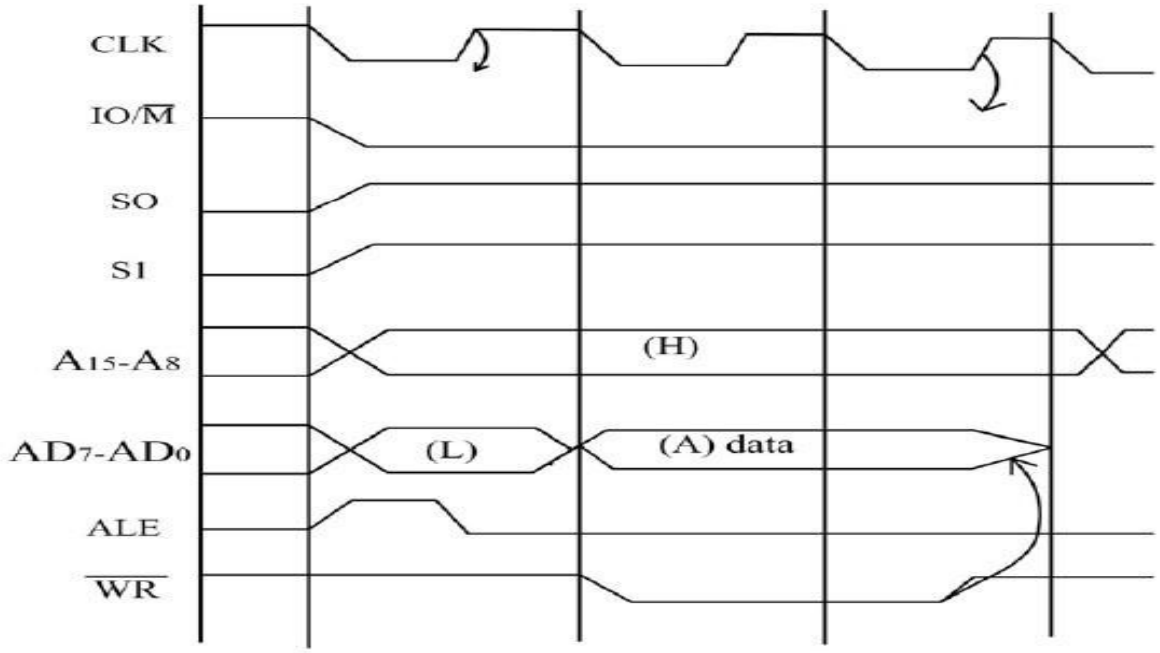
5. The microprocessor has to fetch (read) the data from memory or input device for processing and after processing, it has to store (write) the data to memory or output device. Hence the data bus is bi- directional.
6. The data conditions, after arithmetic or logical operations, are indicated by setting or resetting the flip- flops called flags.
7. The ALE signal goes high at the beginning of each machine cycle indicating the availability of the
address on the address bus, and the signal is used to latch the low order address bus. The IO/M signal is a status signal indicating whether the machine cycle is I/O or memory operation. The IO/M signal iscombined with the RD and WR control signals to generate IOR, IOW, MEMW, MEMR
8. In pipelined architecture the processor will have number of functional units and the execution times of
functional units are overlapped. Each functional unit works independently most of the time.
9. 8085 operate 8bit data. The 8085 has 16 address lines, hence it can access (2^{16}) 64 Kbytes of memory.
10. The 8085 has five flags and they are Carry Flag (CF), Overflow Flag (OF), Parity Flag (PF), Auxiliary carry Flag (AF), Zero Flag (ZF).

C. Long Answer Types Questions:

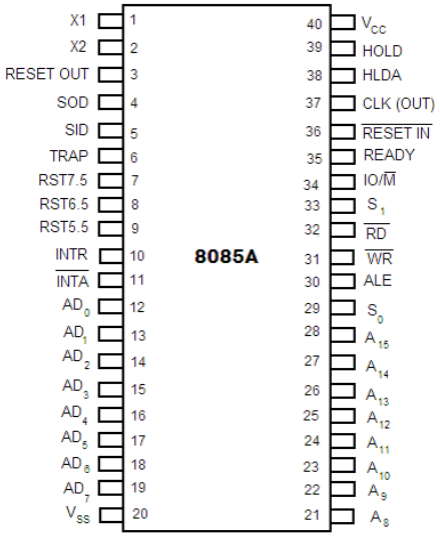
1. Internal architecture of microprocessor 8085



2. Memory Write machine cycle



3. Pin Diagram and Pin description of 8085



8085 is a 40 pin IC, The signals from the pins can be grouped as follows

- Power supply and clock signals
- Address bus
- Data bus
- Control and status signals
- Interrupts and externally initiated signals
- Serial I/O ports

Power supply and Clock frequency signals:

Vcc: + 5 volt power supply

Vss: Ground

X1, X2 : Crystal or R/C network or LC network connections to set the frequency of internal clock generator. The frequency is internally divided by two. Since the basic operating timing frequency is 3 MHz, a 6 MHz crystal is connected externally. CLK (output)-Clock Output is used as the system clock for peripheral and devices interfaced with the microprocessor.

Address Bus:

A8 - A15: (output; 3-state)

It carries the most significant 8 bits of the memory address or the 8 bits of the I/O address.

Data bus:

AD0 - AD7 (input/output; 3-state)

These multiplexed set of lines used to carry the lower order 8 bit address as well as data bus.

- During the opcode fetch operation, in the first clock cycle, the lines deliver the lower order address A0 - A7. •In the subsequent IO / memory, read / write clock cycle the lines are used as data bus.
- The CPU may read or write out data through these lines.

Control and Status signals:

ALE (output) - Address Latch Enable.

- It is an output signal used to give information of AD0-AD7 contents.
- It is a positive going pulse generated when a new operation is started by uP.
- When pulse goes high it indicates that AD0-AD7 are address.
- When it is low it indicates that the contents are data.

RD (output 3-state, active low)

- Read memory or IO device.
- This indicates that the selected memory location or I/O device is to be read and that the data bus is ready for accepting data from the memory or I/O device

WR (output 3-state, active low)

- Write memory or IO device.
- This indicates that the data on the data bus is to be written into the selected memory location or I/O Devices.

IO/M (output) - Select memory or an IO device.

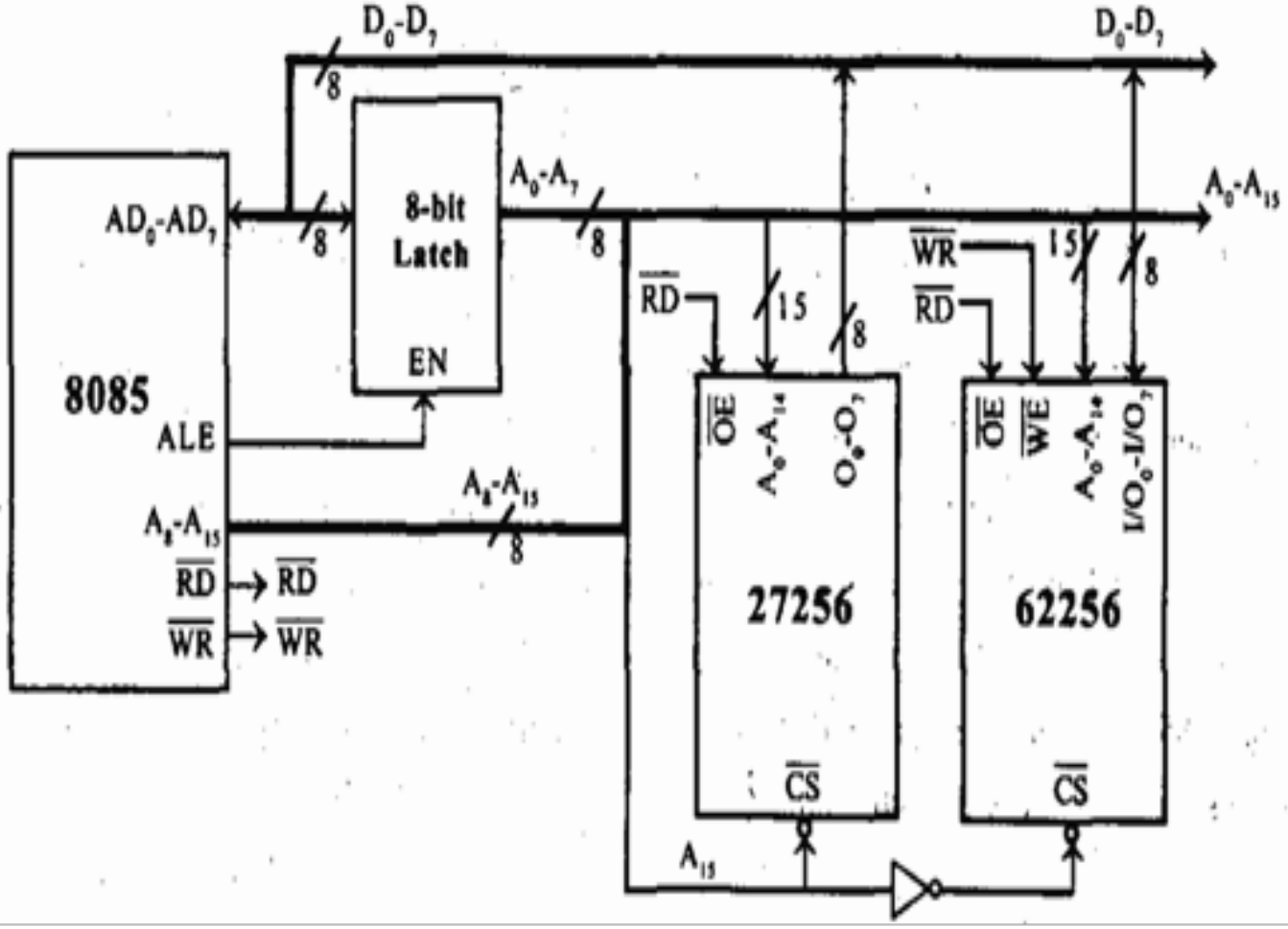
This status signal indicates that the read / write operation relates to whether the memory or I/O device.

It goes high to indicate an I/O operation.

It goes low for memory operations

4. Consider a system in which the available 64kb memory space is equally divided between EPROM and RAM. Interface the EPROM and RAM with 8085 processor.

- Implement 32kb memory capacity of EPROM using single IC 27256.
- 32kb RAM capacity is implemented using single IC 62256.
- The 32kb memory requires 15 address lines and so the address lines A0 - A14 of the processor are connected to 15 address pins of both EPROM and RAM.
- The unused address line A15 is used as to chip select. If A15 is 1, it select RAM and If A15 is 0, it select EPROM.
- Inverter is used for selecting the memory.
- The memory used is both Ram and EPROM, so the low RD and WR pins of processor are connected to low WE and OE pins of memory respectively.
- The address range of EPROM will be 0000H to 7FFFH and that of RAM will be 7FFFH to FFFFH. Two sets of above procedure is used for 64kb of EPROM and RAM.



5. .Assembly program

```
ASSUME CS: CODE, DS: DATA
DATA SEGMENT
NUM1 DW 1234
NUM2 DW 4567
SUM DW ?
DATA ENDS
CODE SEGMENT
START: MOV AX, DATA
MOV DS,AX
MOV AX, NUM1
ADD AX, NUM2
MOV SUM, AX
INT 03H
CODE ENDS
END START
END.
```